

Fig. 1A

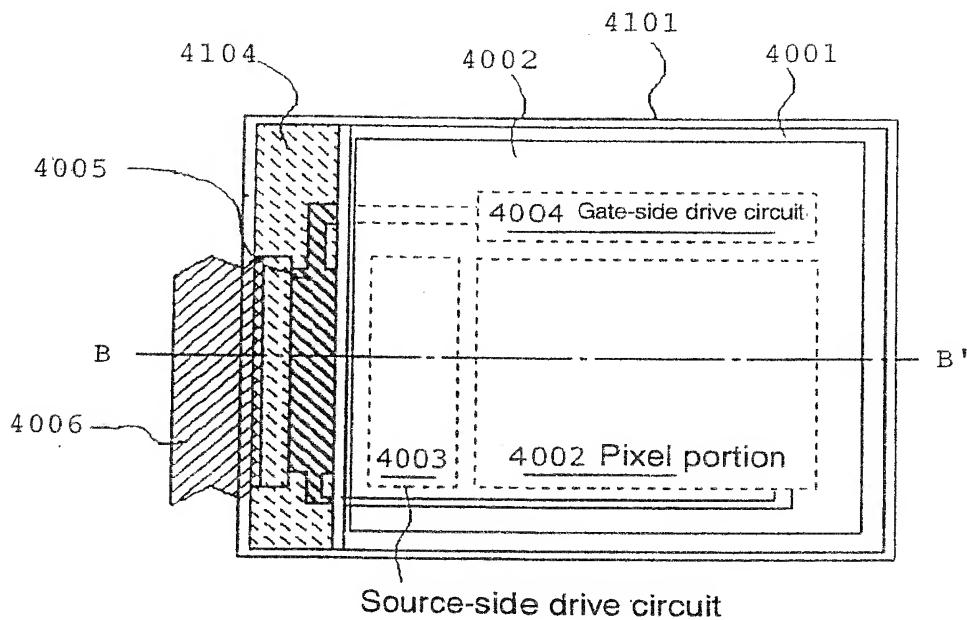
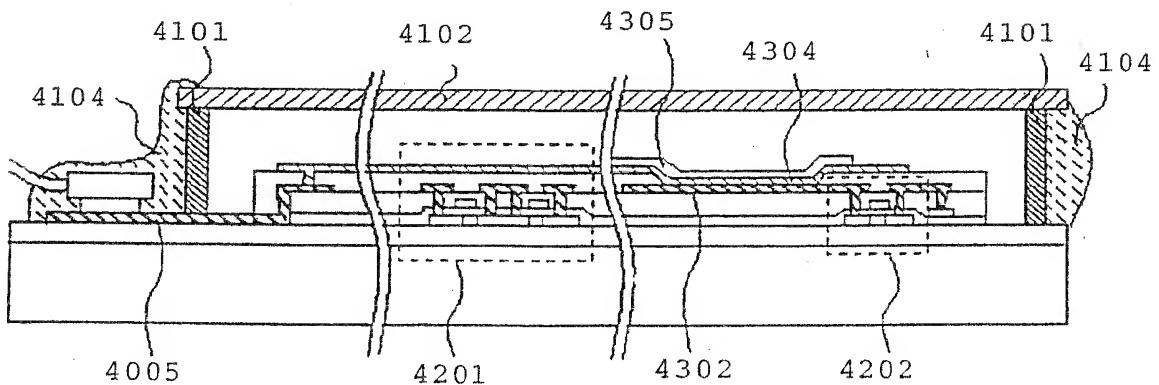


Fig. 1B



PRIOR ART

Fig. 2A

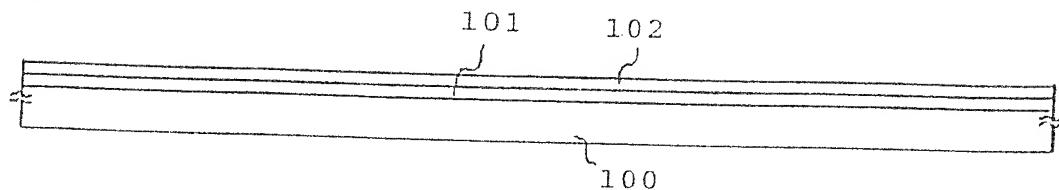


Fig. 2B

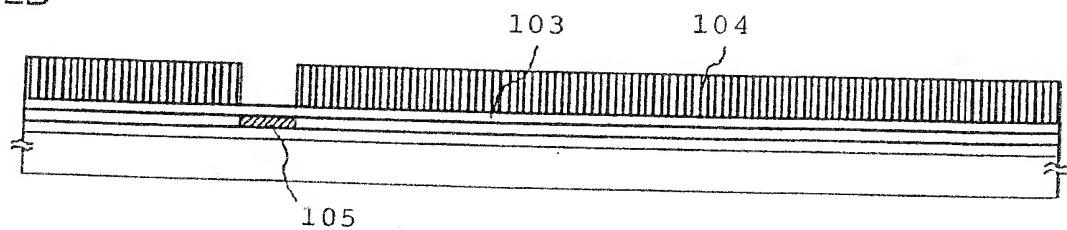


Fig. 2C

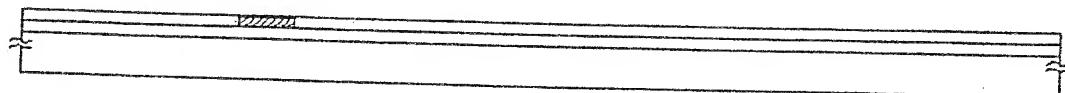


Fig. 2D

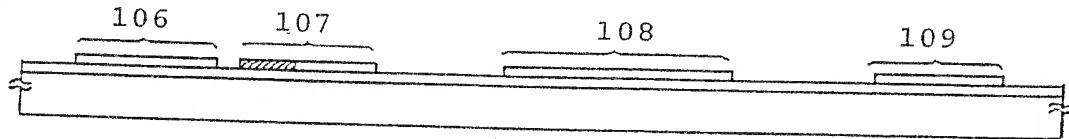
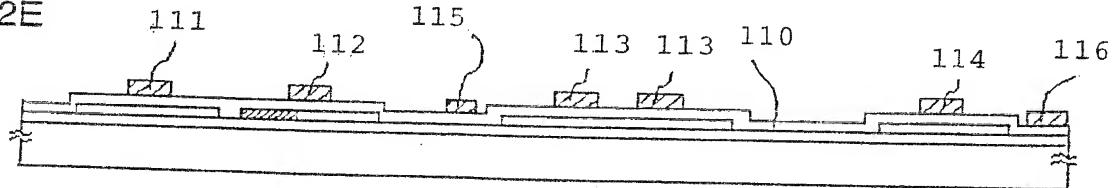
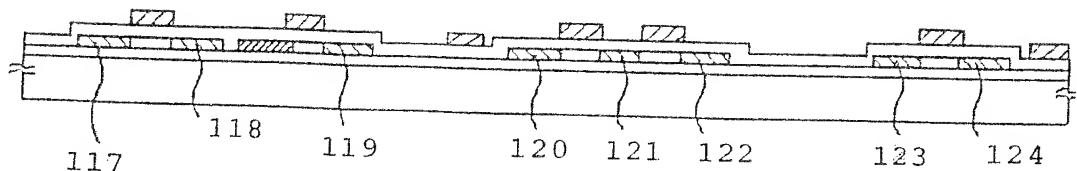


Fig. 2E



PRIOR ART

Fig. 3A



|Fig. 3B

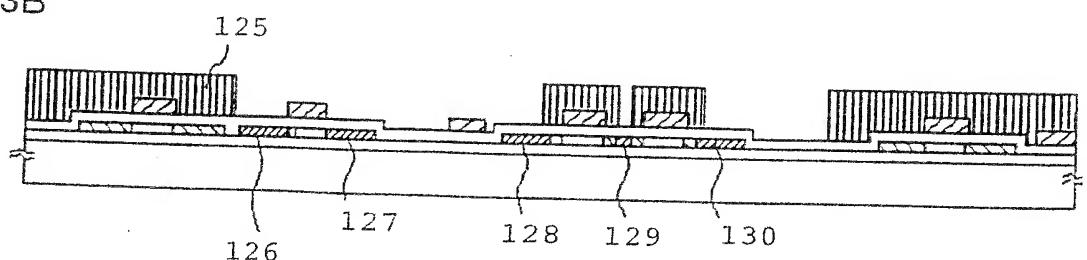


Fig. 3C

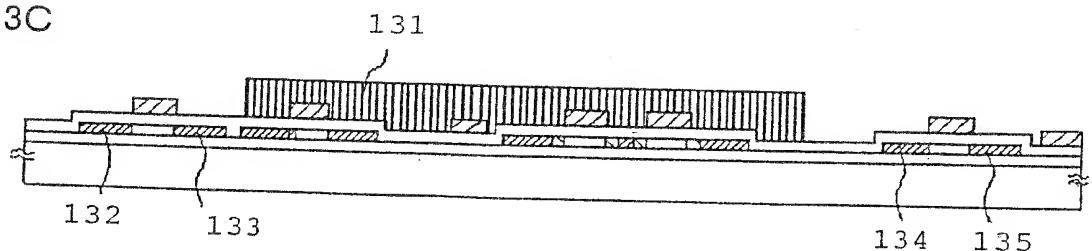
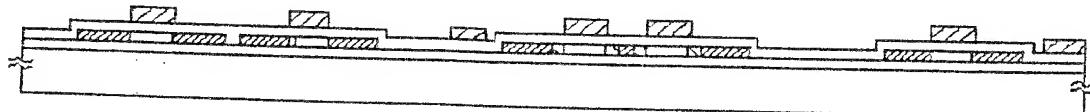


Fig. 3D



PRIOR ART

Fig. 4A

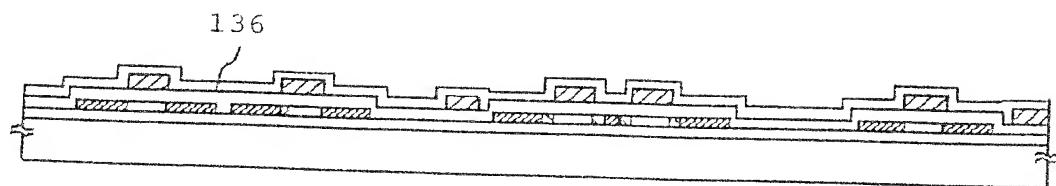


Fig. 4B

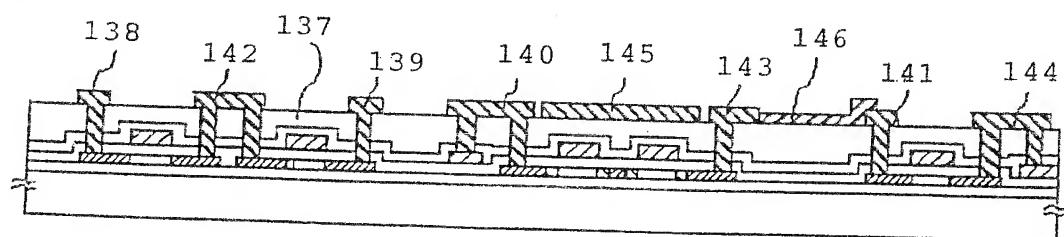
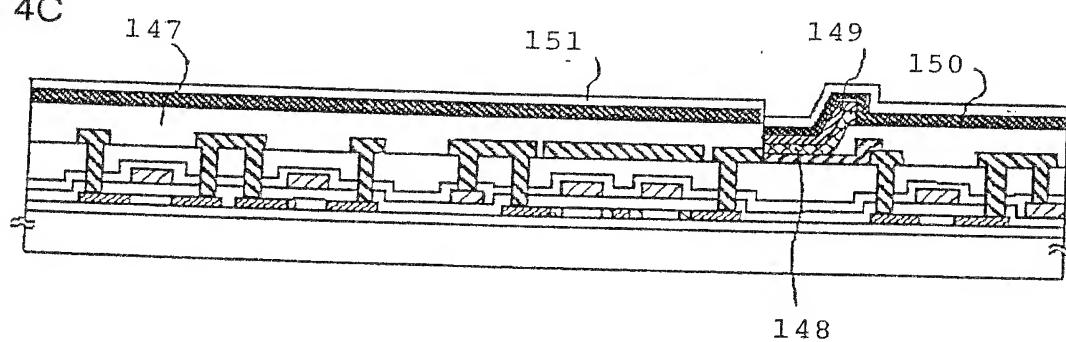


Fig. 4C



PRIOR ART

Fig. 5

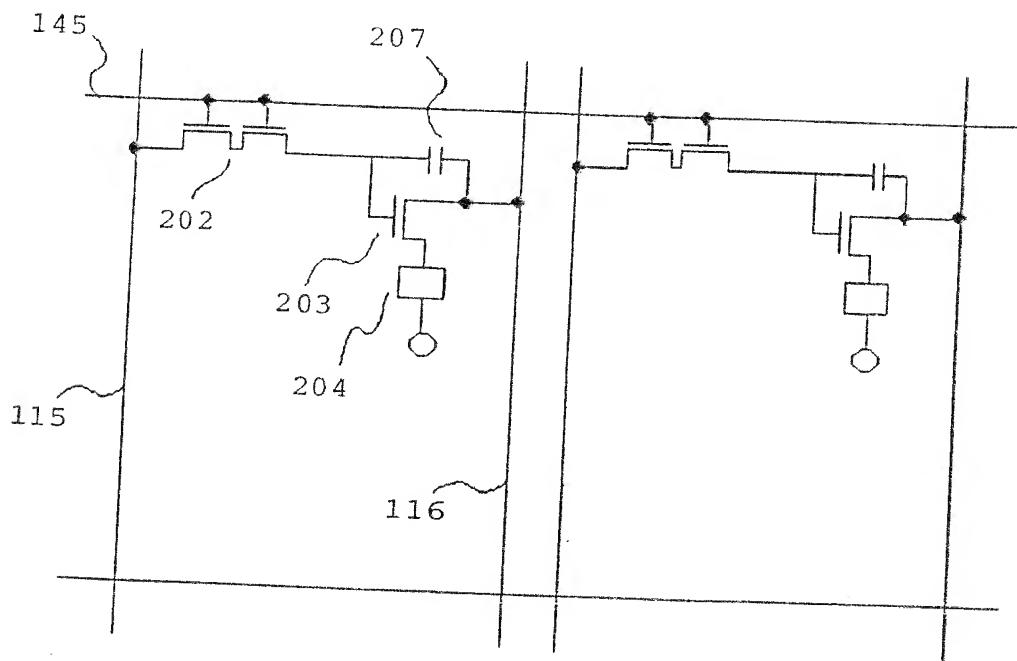
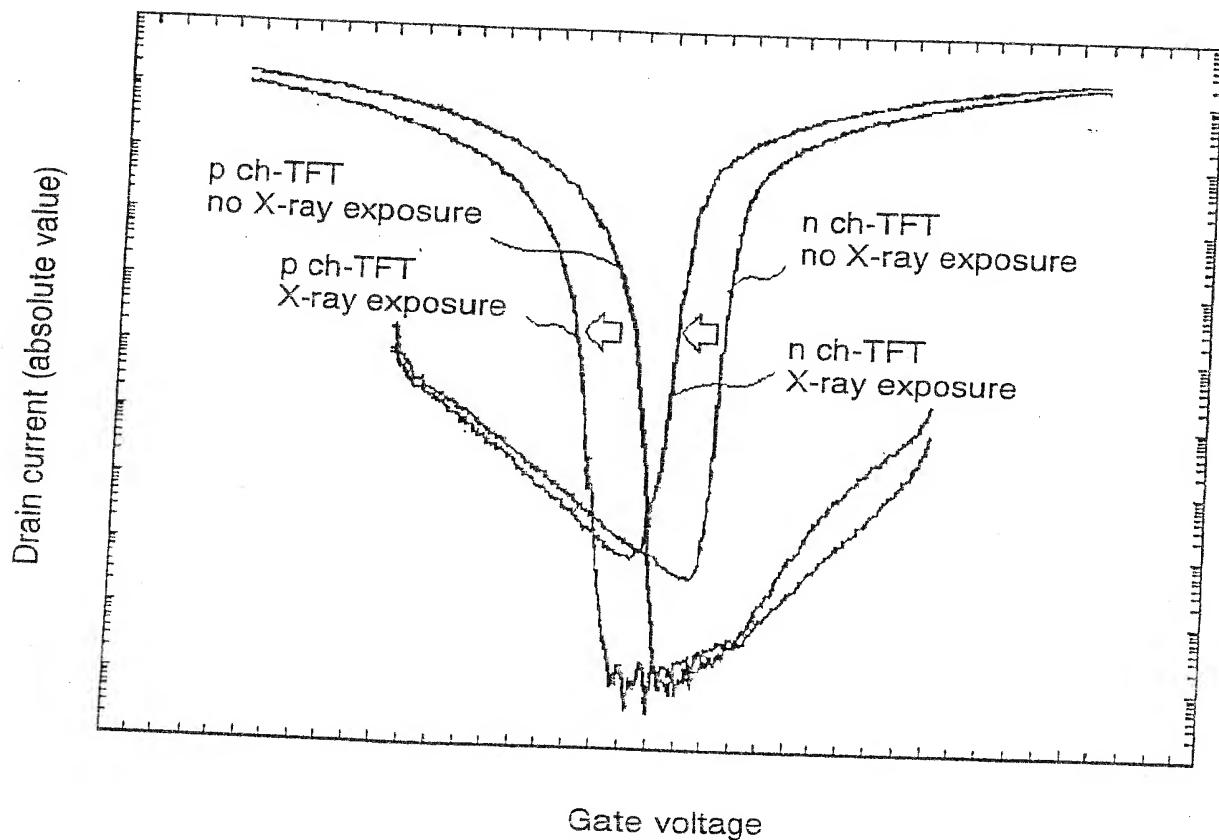


Fig. 6



Gate voltage

Fig. 7A

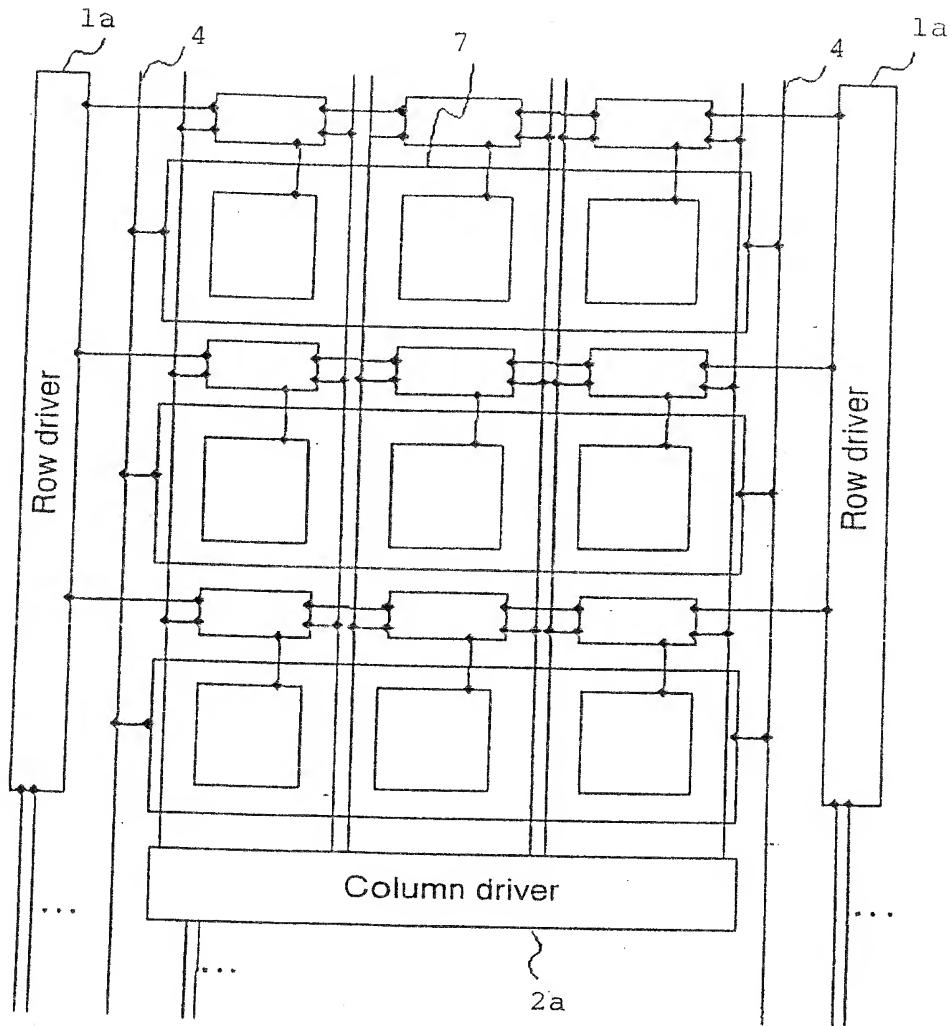


Fig. 7B

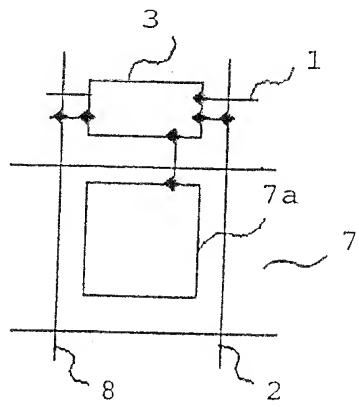


Fig. 8

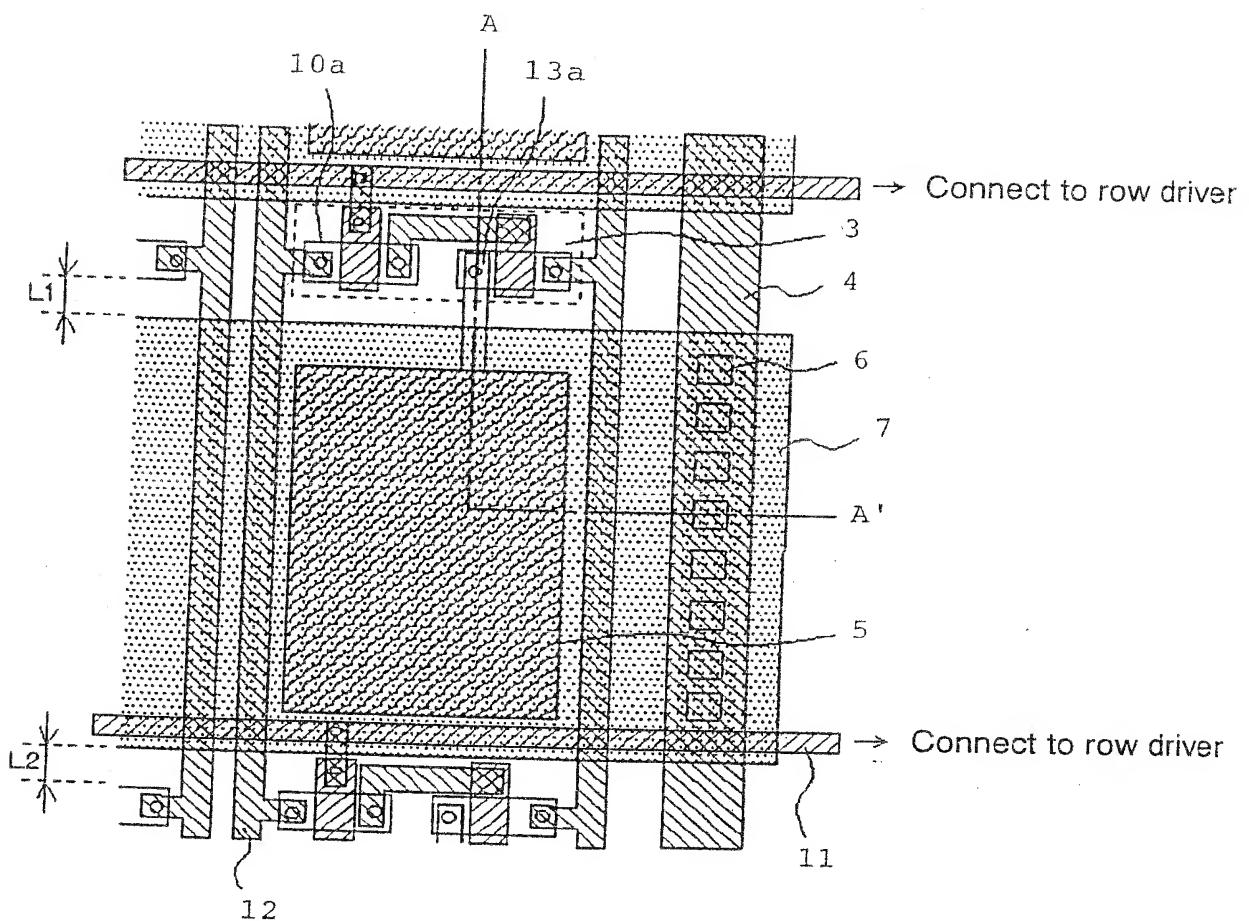


Fig. 9A

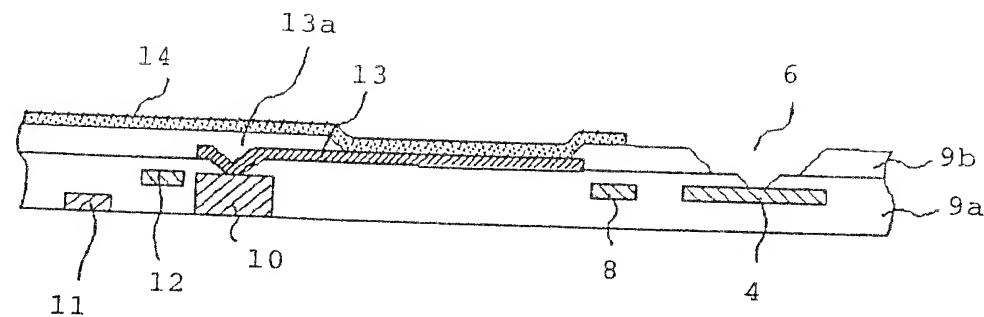


Fig. 9B

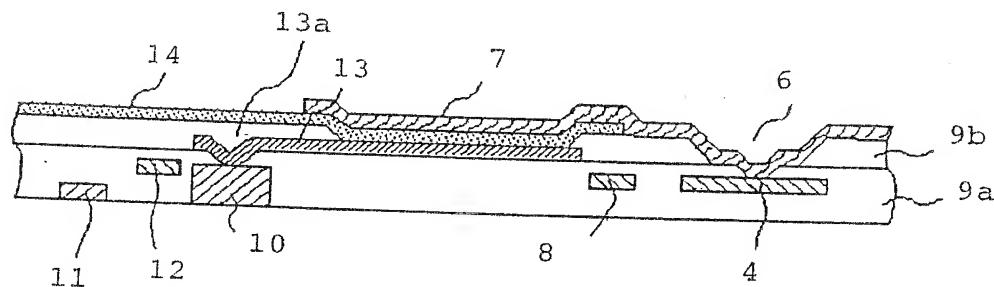


Fig. 10

